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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,135	12/01/2003	Hermann Ruckerbauer	INF-117	1211

48154 7590 12/15/2006

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,135	RUCKERBAUER ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-8 and 10-19 are pending in the present application. This action is in response to the amendment filed 9/11/06.

Drawings

The replacement drawings were received on 9/11/06. These drawings are unacceptable. Although applicant has labeled some of the elements in the replacement sheets, there are some numbered elements that are not labeled on the replacement drawing. Examples: Figure 1 – elements 1, 5, 3 and/or 61 (it is unclear which element the redundant memory is labeling) 62, and 63. The same part numbers are not labeled throughout the remainder of the figures. The drawings are objected to because descriptive labels other than numerical are needed for figures 1-5. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Figures 1and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 15 is objected to because of the following informalities: line 1 of claim 15 states; "The buffer and error checking module of claims 13" In this instance 'claims' should read 'claim'. Appropriate correction is required.

Claim 19 is objected to because of the following informalities: "developing, on the basis of an analysis of transfer errors occurring between the memory control device and the memory module, a bus system of respective precursor systems in a direction of a minimum number of transfer errors;" is not clear what is being done

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 18 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18: The phrase "an occurrence of a data error in the data" is unclear which 'data' that 'the data' is referencing.

Claim 19:"developing, on the basis of an analysis of transfer errors occurring between the memory control device and the memory module, a bus system of

respective precursor systems in a direction of a minimum number of transfer errors;" is unclear, and should be clarified as to what is specifically being claimed by the term 'developing' with respect to "in a direction of a minimum number of transfer errors".

The above claims will not be further considered with respect to prior art in this office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8 and 10-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's admitted prior art (AAPA) in the background of the present application.

As per claim 1, AAPA teach a memory module with a plurality of data memory devices for storing data, the data memory devices are configured as DRAM modules pp [0004]; at least one buffer device connected to the data memory devices by at least data lines, and serving to condition at least data signals, the data signals being transferred on the data lines between the data memory devices and a memory control device of the data memory system pp [0006]; and at least one buffer and error checking

module, which in each case integrates a buffer device and a data memory device for storing redundancy data operable to detect and to correct erroneous data in a common device housing pp [0007].

As per claim 2, AAPA teach each of the buffer and error checking modules is connected to an even number of data memory devices for storing the data (see Figure 1).

As per claim 3, AAPA teach the data memory devices are arranged symmetrically with respect to the buffer and error checking module (see Figure 1).

As per claim 4, AAPA teach the buffer and error checking module has an error detecting unit operable to perform the following: during a transfer of data to the memory module, to form and to store the redundancy data and during a transfer of data to the memory control device, to form check data from the data and also to compare respectively corresponding redundancy data and with the check data pp [0007].

As per claim 5, AAPA teach the buffer and error checking module has an error correction unit operable to correct erroneous data on the basis of respectively corresponding redundancy data and check data pp [0006-0007].

As per claim 6, AAPA teach error correction is performed exclusively on the memory module and without communication with the memory control device pp [0007].

As per claim 7, AAPA teach the memory module has an error signaling unit operable to transfer information on error events to the memory control device pp [0007].

As per claim 8, AAPA teach the buffer and error checking module has an error evaluation trait operable to identify and to mask out defective memory cells in the data memory devices pp [0009].

As per claim 10, AAPA teach the data memory devices comprise a DDR interface pp [0004].

As per claim 11, AAPA teach the maximum dimensions of the memory module are about 1.2 inches x 5.25 inches pp [0017].

As per claim 12, AAPA teach a buffer and error checking module for memory modules, the memory modules having a plurality of DRAM devices operated in data memory systems pp [0004], the buffer and error checking module having connecting devices pp [0006]; a buffer/redriver formed in a semiconductor substrate and operable to condition at least data signals that are transferred to and from the memory modules

pp [0006]; and a memory cell array formed in the semiconductor substrate as an error data memory pp [0007].

As per claim 13, AAPA teach an error detecting unit operable, during a transfer of data to the memory module, to form and to store redundancy data and, during a transfer of data to a memory control device of the data memory system, to compare the stored redundancy data with check data formed from the data to be transferred pp [0007-0009].

As per claim 14, AAPA teach an error correction unit operable to correct erroneous data on the basis of respectively corresponding redundancy data and check data pp [0007].

As per claim 15, AAPA teach an error signaling unit operable to transfer information on error events to the data memory system pp [0007].

As per claim 16, AAPA teach an error evaluation unit operable to identify and to mask out defective memory cells in data memory devices connected to the buffer and error checking module pp [0009].

As per claim 17, AAPA teach a method for operating a memory module having a plurality of DRAM devices for storing data and at least one buffer and error checking

module in a data memory system pp [0004], the method comprising: receiving data signals of data transferred to the memory module and conditioning the data signals with the buffer and error checking module pp [0006]; forming, in the buffer and error checking module, a corresponding set of redundancy data with respect to the data; storing the data in the DRAM devices pp [0007]; storing the respectively corresponding set of redundancy data in the buffer and error checking module; forming in the buffer and error checking module, during a transfer of stored data from the DRAM devices to a memory control device of the data memory system, a corresponding set of check data; detecting, through a comparison of respectively corresponding redundancy data and check data, data errors that have occurred in the data are and correcting any such errors on a case by case basis; and transferring corrected data to the memory control device pp [0007-0009].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miura et al. U.S. Patent No. 6,791,877.

This patent teaches a semiconductor device which includes a large capacity non-volatile memory and at least one random access memory, said the access time of said device being matched to the access time of each random access memory. The semiconductor memory device is comprised of: a non-volatile memory FLASH having a

first reading time; a random access memory DRAM having a second reading time which is more than 100 times shorter than the first reading time; a circuit that includes a control circuit connected to both the FLASH and the DRAM and enabled to control accesses to those FLASH and DRAM; and a plurality of I/O terminals connected to the circuit. As a result, FLASH data is transferred to the DRAM before the DRAM is accessed, thereby matching the access time between the FLASH and the DRAM. Data is written back from the DRAM to the FLASH as needed, thereby keeping data matched between the FLASH and the DRAM and storing the data.

The examiner would like to point out that it was the translation error of the term useful data that led to confusion initially and although this has been clarified and placed in the record of the case, the examiner suggests that the term useful data within the specification be corrected in order to clarify the invention to a person reading this application in the future. Also, the claimed invention should be particularly pointed out and distinctly claimed in order to not be so vague as to read on the background of the invention or the above cited prior art. The examiner invites applicant to call and set up an interview to discuss the claim language in order to clarify this invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

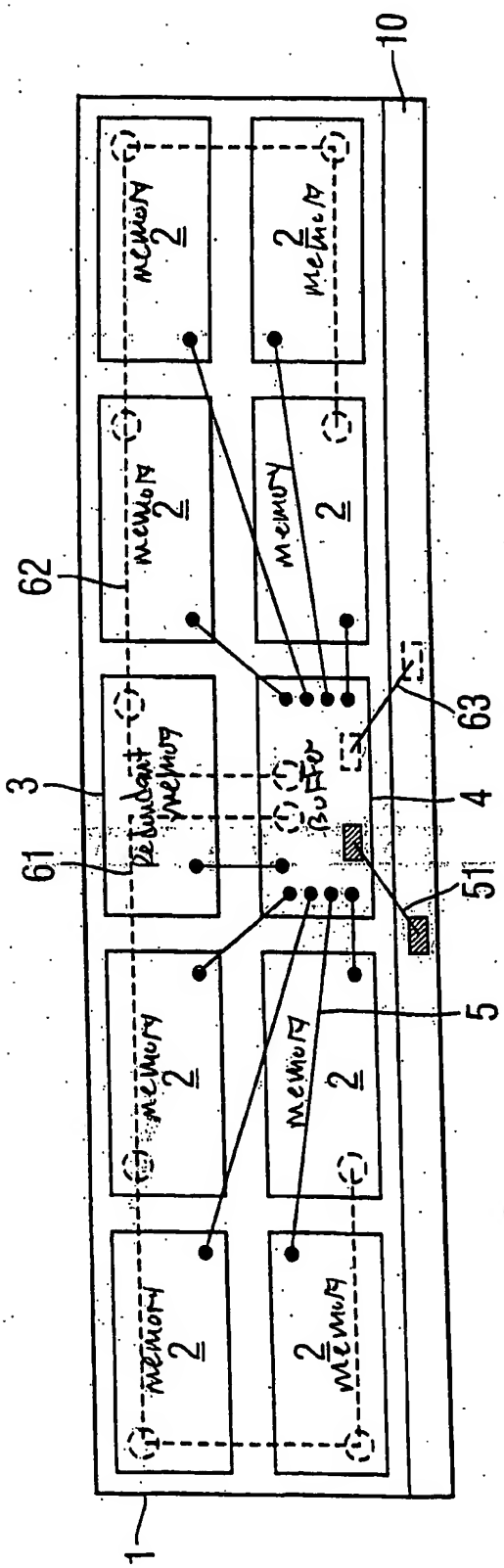
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138

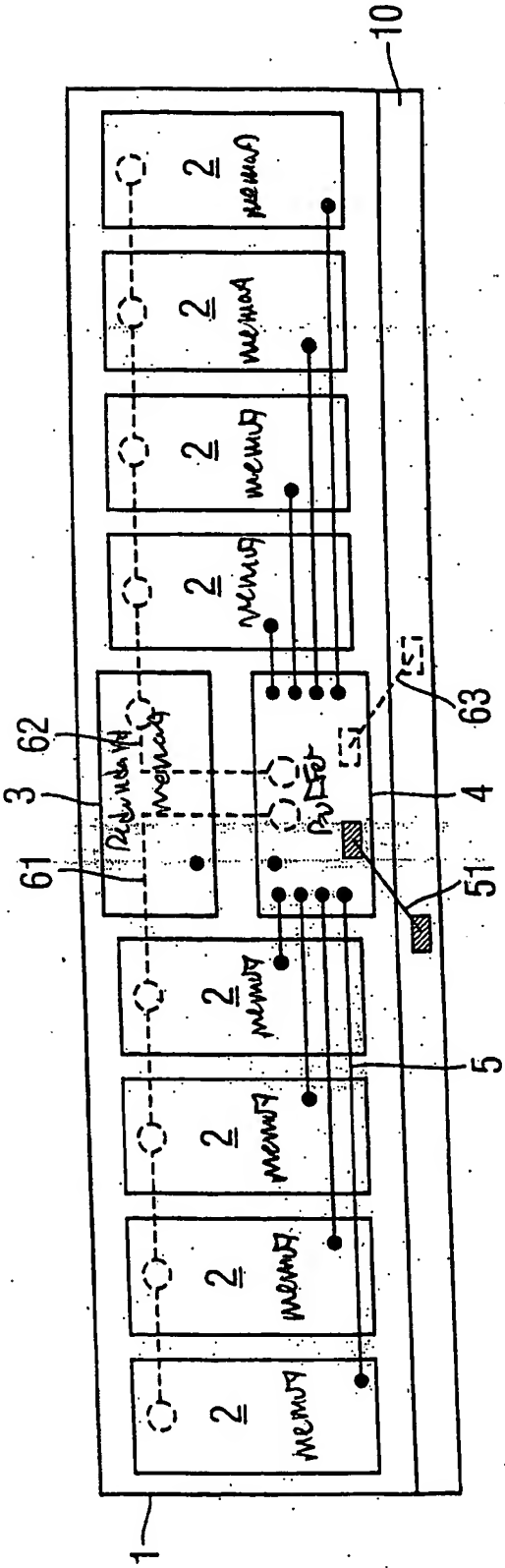
REPLACEMENT SHEET

FIG 1



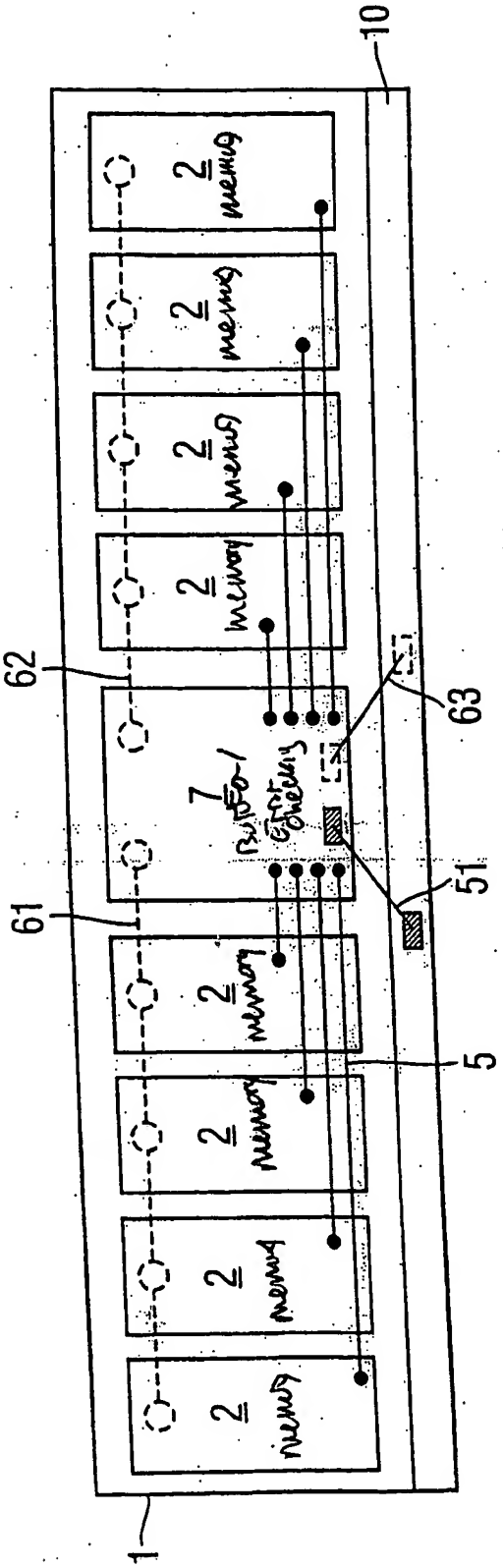
REPLACEMENT
SHEET

FIG 2



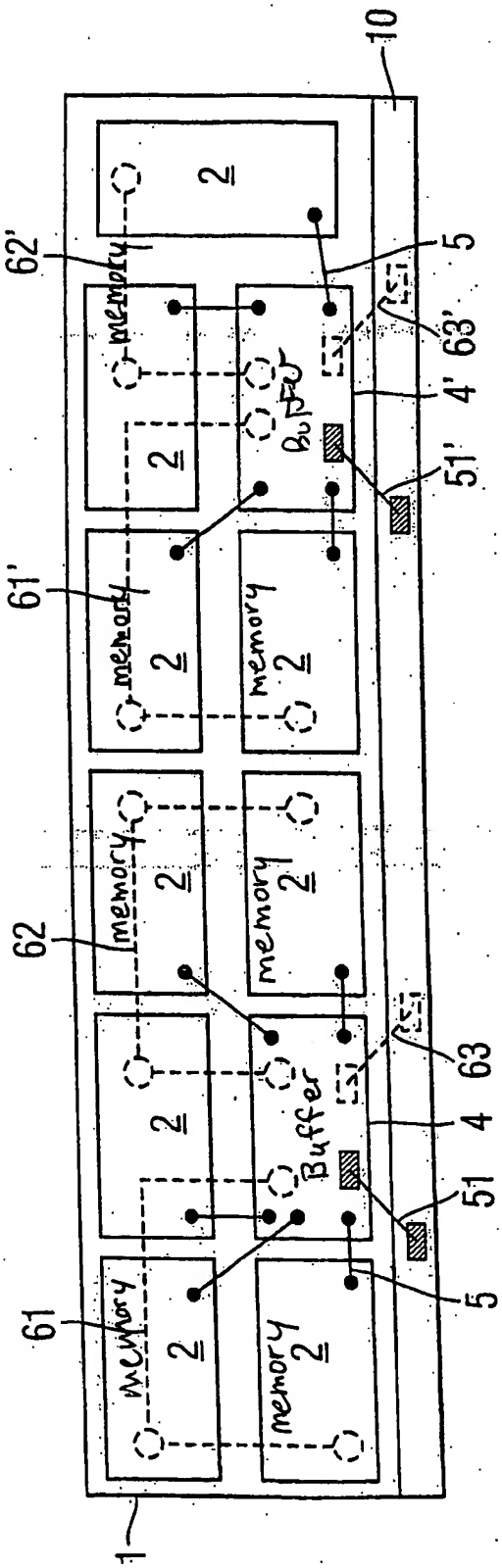
REPLACEMENT
SHEET

FIG 3



REPLACEMENT
SHEET

FIG 4



REPLACEMENT
SHEET

FIG 5